

**SINGLE-CHANNEL
6N137
HCPL-2601
HCPL-2611**

**DUAL-CHANNEL
HCPL-2630
HCPL-2631**

DESCRIPTION

The 6N137, HCPL-2601/2611 single-channel and HCPL-2630/2631 dual-channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photodetector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

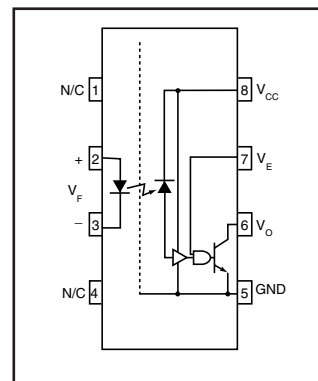
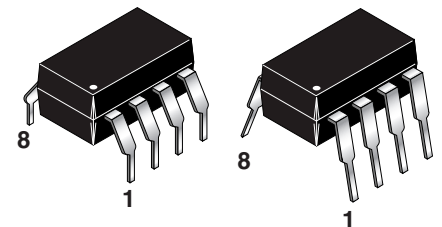
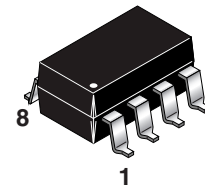
An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The HCPL-2601 and HCPL-2631 has a minimum CMR of 5 kV/μs. The HCPL-2611 has a minimum CMR of 10 kV/μs.

FEATURES

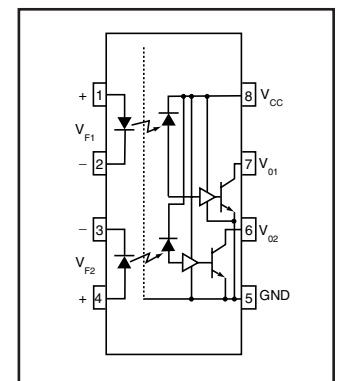
- Very high speed-10 MBit/s
- Superior CMR-10 kV/μs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)

APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface



6N137
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TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

A 0.1 μF bypass capacitor must be connected between pins 8 and 5.
(See note 1)

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ABSOLUTE MAXIMUM RATINGS (No derating required up to 85°C)

Parameter	Symbol	Value	Units
Storage Temperature	T_{STG}	-55 to +125	°C
Operating Temperature	T_{OPR}	-40 to +85	°C
Lead Solder Temperature	T_{SOL}	260 for 10 sec	°C
EMITTER			
DC/Average Forward Current	I_F	50	mA
Input Current		30	
Enable Input Voltage	V_E	5.5	V
Not to exceed V_{CC} by more than 500 mV			
Reverse Input Voltage	V_R	5.0	V
Power Dissipation	P_I	100	mW
		45	
DETECTOR			
Supply Voltage	V_{CC} (1 minute max)	7.0	V
Output Current	I_O	50	mA
		50	
Output Voltage	V_O	7.0	V
Collector Output Power Dissipation	P_O	85	mW
		60	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}	*6.3	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Enable Voltage, Low Level	V_{EL}	0	0.8	V
Enable Voltage, High Level	V_{EH}	2.0	V_{CC}	V
Low Level Supply Current	T_A	-40	+85	°C
Fan Out (TTL load)	N		8	

* 6.3 mA is a guard banded value which allows for at least 20 % CTR degradation. Initial input current threshold value is 5.0 mA or less

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ELECTRICAL CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
EMITTER	($I_F = 10\text{ mA}$)				1.8	
Input Forward Voltage	$T_A = 25^\circ\text{C}$	V_F		1.4	1.75	V
Input Reverse Breakdown Voltage	($I_R = 10\ \mu\text{A}$)	B_{VR}	5.0			V
Input Capacitance	($V_F = 0$, $f = 1\text{ MHz}$)	C_{IN}		60		pF
Input Diode Temperature Coefficient	($I_F = 10\text{ mA}$)	$\Delta V_F/\Delta T_A$		-1.4		mV/°C
DETECTOR						
High Level Supply Current	Single Channel ($V_{CC} = 5.5\text{ V}$, $I_F = 0\text{ mA}$) Dual Channel ($V_E = 0.5\text{ V}$)	I_{CCH}		7	10	mA
Low Level Supply Current	Single Channel ($V_{CC} = 5.5\text{ V}$, $I_F = 10\text{ mA}$) Dual Channel ($V_E = 0.5\text{ V}$)	I_{CCL}		9	13	mA
Low Level Enable Current	($V_{CC} = 5.5\text{ V}$, $V_E = 0.5\text{ V}$)	I_{EL}		-0.8	-1.6	mA
High Level Enable Current	($V_{CC} = 5.5\text{ V}$, $V_E = 2.0\text{ V}$)	I_{EH}		-0.6	-1.6	mA
High Level Enable Voltage	($V_{CC} = 5.5\text{ V}$, $I_F = 10\text{ mA}$)	V_{EH}	2.0			V
Low Level Enable Voltage	($V_{CC} = 5.5\text{ V}$, $I_F = 10\text{ mA}$) (Note 3)	V_{EL}			0.8	V

SWITCHING CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $I_F = 7.5\text{ mA}$ Unless otherwise specified.)

AC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Propagation Delay Time to Output High Level	(Note 4) ($T_A = 25^\circ\text{C}$) ($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Fig. 12)	T_{PLH}	20	45	75	ns
Propagation Delay Time to Output Low Level	(Note 5) ($T_A = 25^\circ\text{C}$) ($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Fig. 12)	T_{PHL}	25	45	75	ns
Pulse Width Distortion	($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Fig. 12)	$ T_{PHL} - T_{PLH} $		3	35	ns
Output Rise Time (10-90%)	($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Note 6) (Fig. 12)	t_r		50		ns
Output Fall Time (90-10%)	($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Note 7) (Fig. 12)	t_f		12		ns
Enable Propagation Delay Time to Output High Level	($I_F = 7.5\text{ mA}$, $V_{EH} = 3.5\text{ V}$) ($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Note 8) (Fig. 13)	t_{ELH}		20		ns
Enable Propagation Delay Time to Output Low Level	($I_F = 7.5\text{ mA}$, $V_{EH} = 3.5\text{ V}$) ($R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) (Note 9) (Fig. 13)	t_{EHL}		20		ns
Common Mode Transient Immunity (at Output High Level)	($T_A = 25^\circ\text{C}$) $ V_{CM} = 50\text{ V}$, (Peak) ($I_F = 0\text{ mA}$, $V_{OH}(\text{Min.}) = 2.0\text{ V}$) 6N137, HCPL-2630 ($R_L = 350\ \Omega$) (Note 10) HCPL-2601, HCPL-2631 (Fig. 14) HCPL-2611 $ V_{CM} = 400\text{ V}$	$ CM_H $		10,000	10,000	V/ μs
Common Mode Transient Immunity (at Output Low Level)	($R_L = 350\ \Omega$) ($I_F = 7.5\text{ mA}$, $V_{OL}(\text{Max.}) = 0.8\text{ V}$) 6N137, HCPL-2630 $ V_{CM} = 50\text{ V}$ (Peak) HCPL-2601, HCPL-2631 ($T_A = 25^\circ\text{C}$) (Note 11) (Fig. 14) HCPL-2611 ($T_A = 25^\circ\text{C}$) $ V_{CM} = 400\text{ V}$	$ CM_L $		10,000	10,000	V/ μs

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TRANSFER CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
High Level Output Current	($V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$) ($I_F = 250\ \mu\text{A}$, $V_E = 2.0\text{ V}$) (Note 2)	I_{OH}			100	μA
Low Level Output Current	($V_{CC} = 5.5\text{ V}$, $I_F = 5\text{ mA}$) ($V_E = 2.0\text{ V}$, $I_{CL} = 13\text{ mA}$) (Note 2)	V_{OL}		.35	0.6	V
Input Threshold Current	($V_{CC} = 5.5\text{ V}$, $V_O = 0.6\text{ V}$, $V_E = 2.0\text{ V}$, $I_{OL} = 13\text{ mA}$)	I_{FT}		3	5	mA

ISOLATION CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-Output Insulation Leakage Current	(Relative humidity = 45%) ($T_A = 25^{\circ}\text{C}$, $t = 5\text{ s}$) ($V_{I-O} = 3000\text{ VDC}$) (Note 12)	I_{I-O}			1.0*	μA
Withstand Insulation Test Voltage	(RH < 50%, $T_A = 25^{\circ}\text{C}$) (Note 12) ($t = 1\text{ min.}$)	V_{ISO}	2500			V_{RMS}
Resistance (Input to Output)	($V_{I-O} = 500\text{ V}$) (Note 12)	R_{I-O}		10^{12}		Ω
Capacitance (Input to Output)	($f = 1\text{ MHz}$) (Note 12)	C_{I-O}		0.6		pF

 ** All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$
NOTES

- The V_{CC} supply to each optoisolator must be bypassed by a $0.1\ \mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
- Each channel.
- Enable Input - No pull up resistor required as the device has an internal pull up resistor.
- t_{PLH} - Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- t_{PHL} - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- t_r - Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- t_f - Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- t_{ELH} - Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- t_{EHL} - Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- CM_H - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0\text{ V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
- CM_L - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the low output state (i.e., $V_{OUT} < 0.8\text{ V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
- Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.

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TYPICAL PERFORMANCE CURVES

Fig. 1 Low Level Output Voltage vs. Ambient Temperature

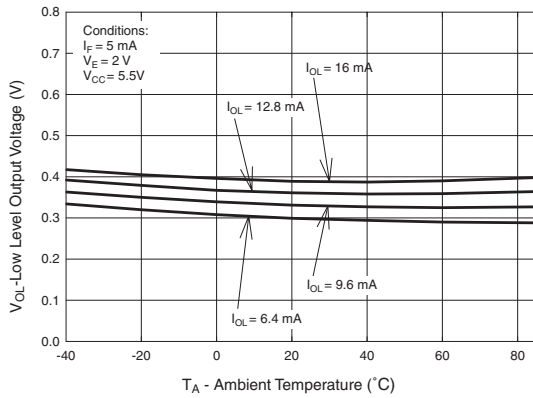


Fig. 2 Input Diode Forward Voltage vs. Forward Current

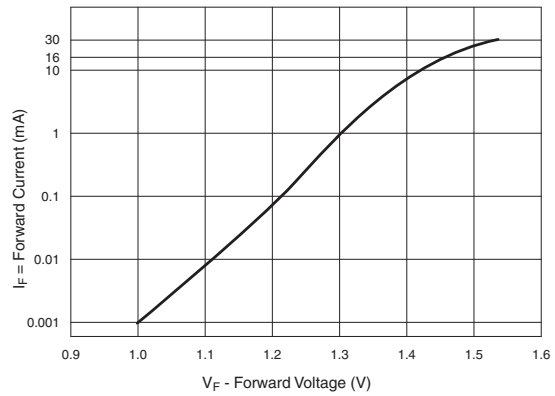


Fig. 3 Switching Time vs. Forward Current

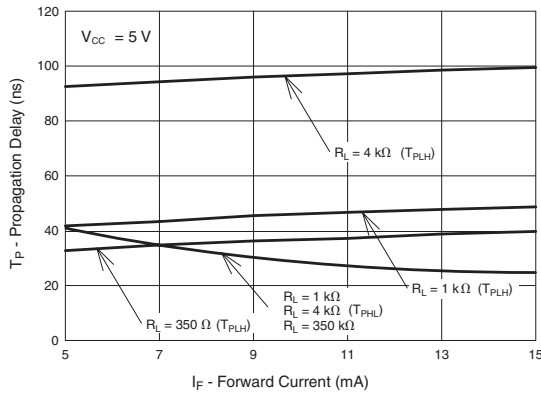


Fig. 4 Low Level Output Current vs. Ambient Temperature

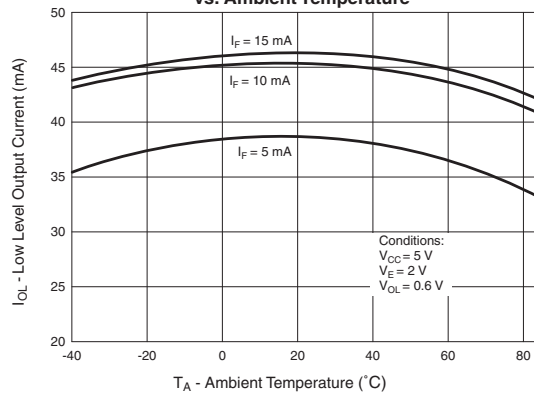


Fig. 5 Input Threshold Current vs. Ambient Temperature

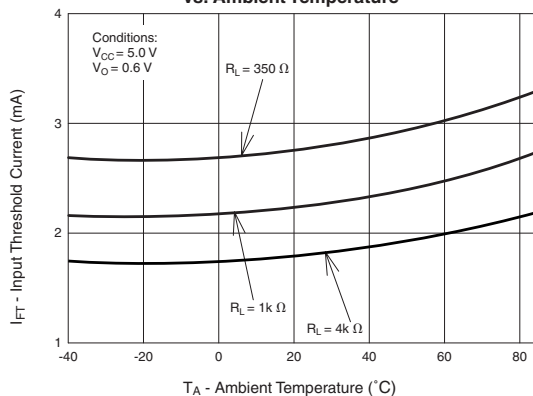
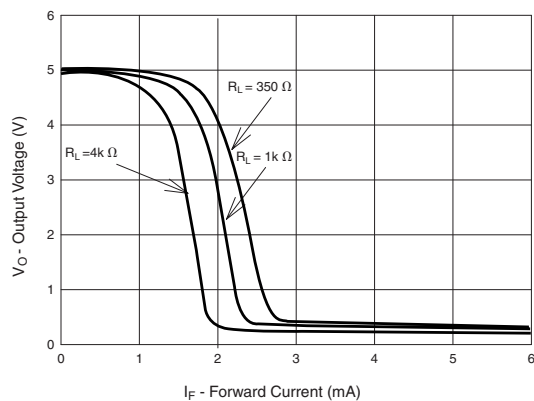


Fig. 6 Output Voltage vs. Input Forward Current



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Fig. 7 Pulse Width Distortion vs. Temperature

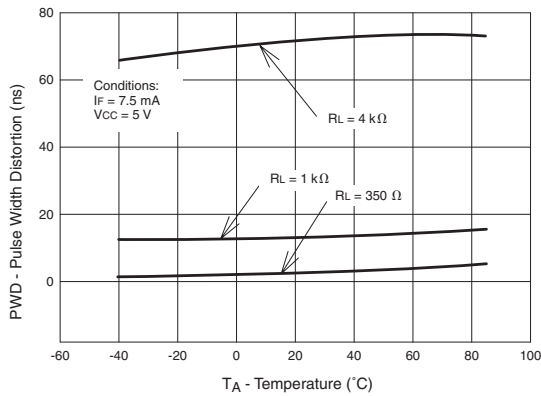


Fig. 8 Rise and Fall Time vs. Temperature

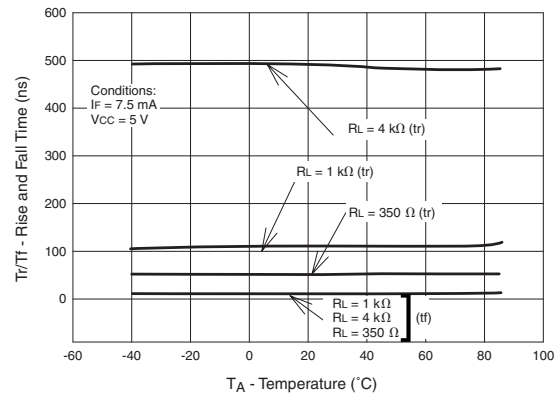


Fig. 9 Enable Propagation Delay vs. Temperature

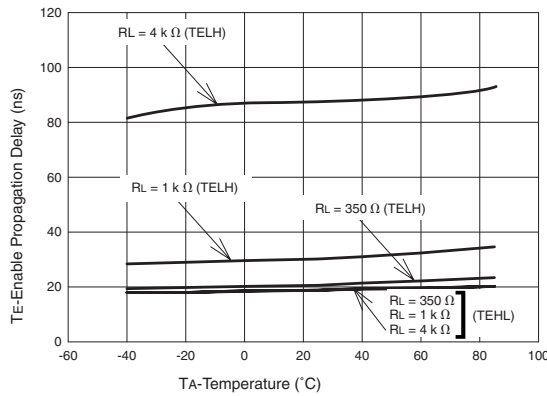


Fig. 10 Switching Time vs. Temperature

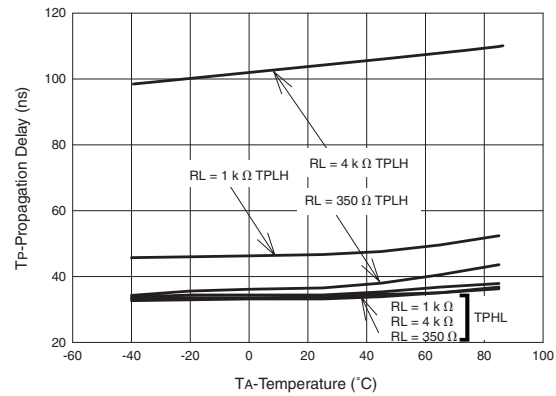
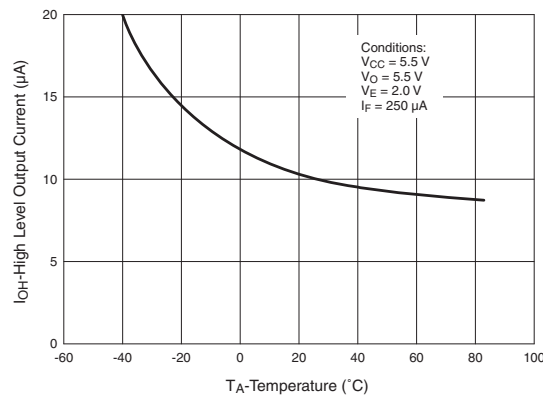


Fig. 11 High Level Output Current vs. Temperature



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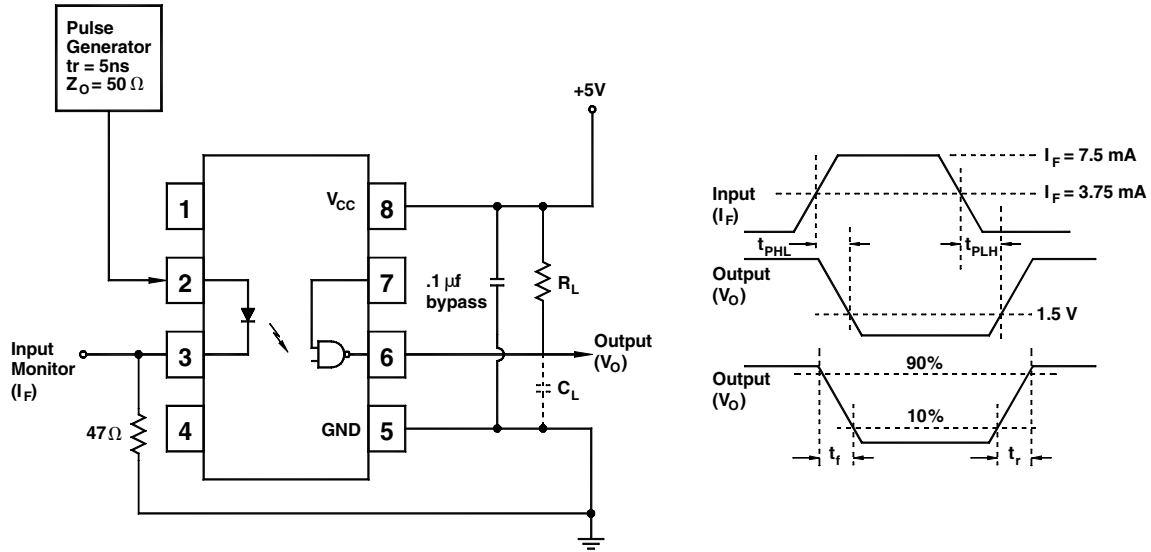


Fig. 12 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f .

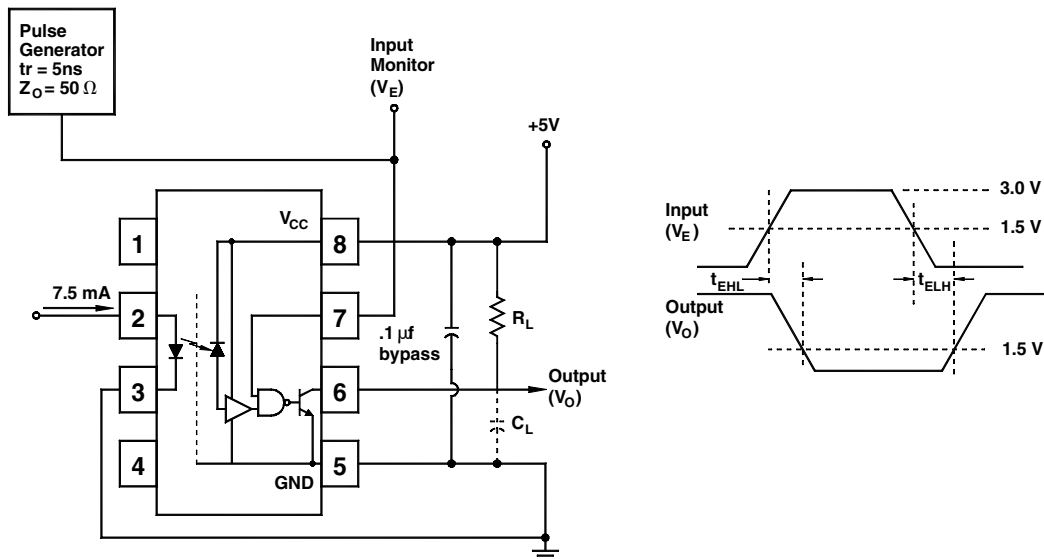


Fig. 13 Test Circuit t_{EHL} and t_{ELH} .

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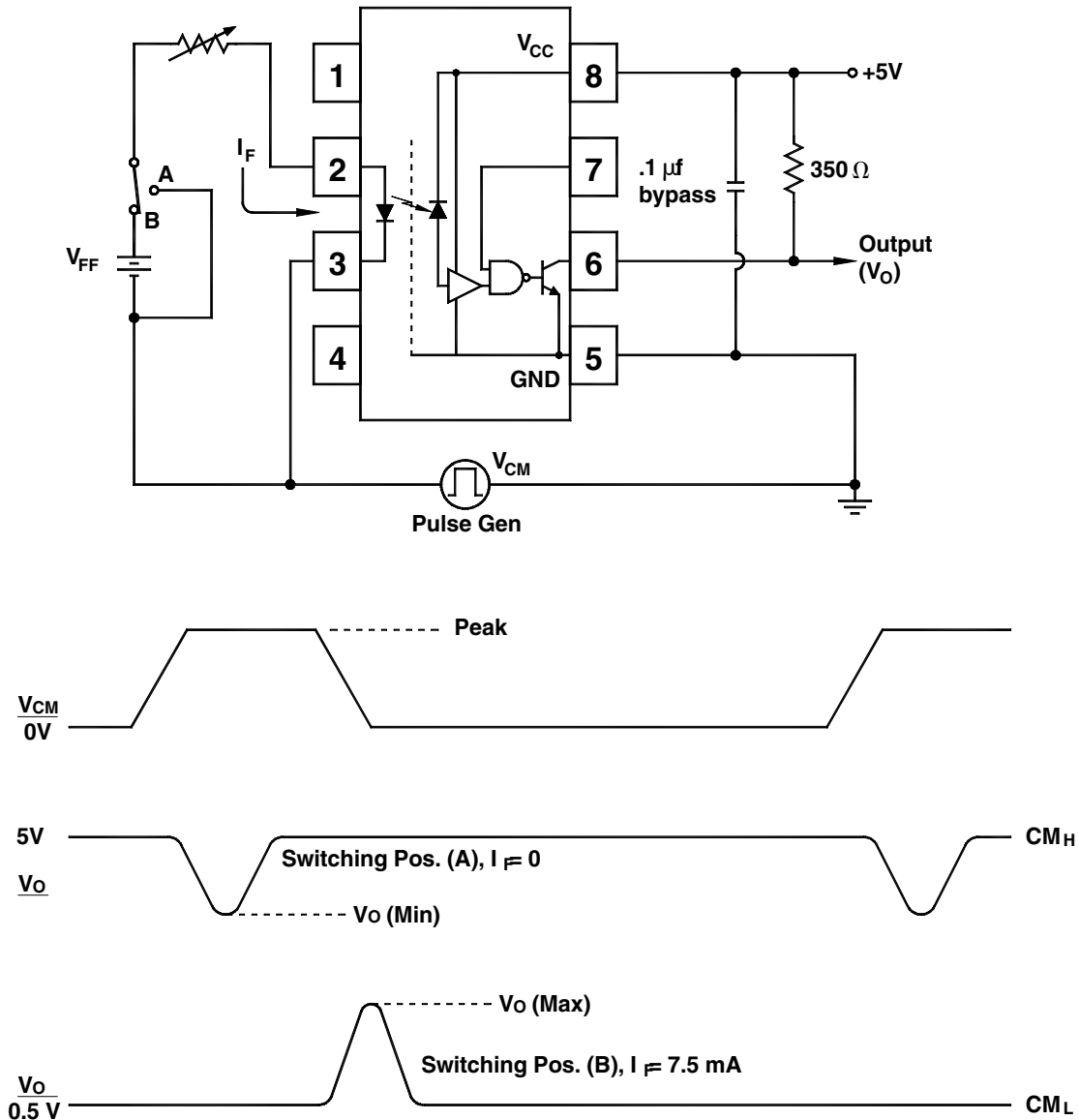
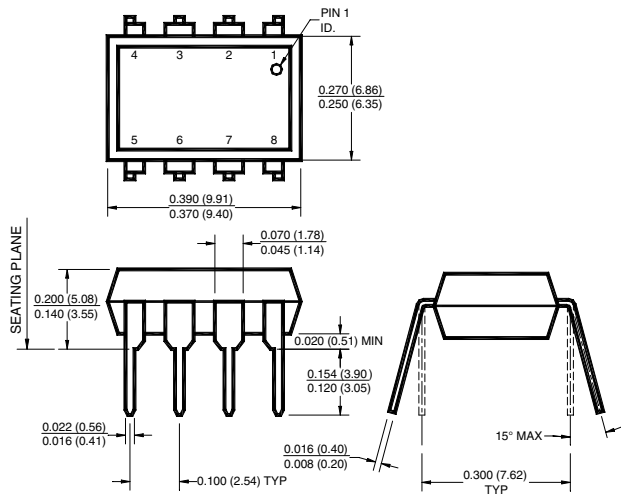


Fig. 14 Test Circuit Common Mode Transient Immunity

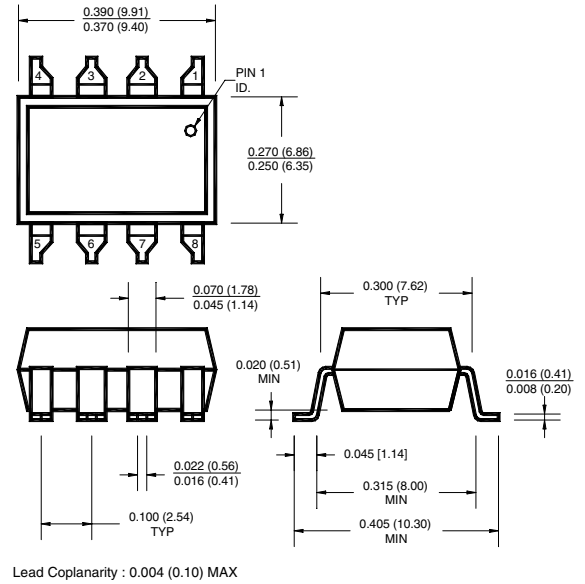
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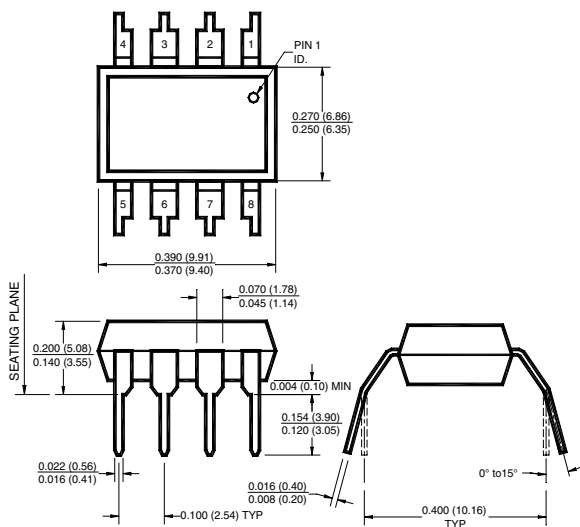
Package Dimensions (Through Hole)



Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



NOTE

All dimensions are in inches (millimeters)

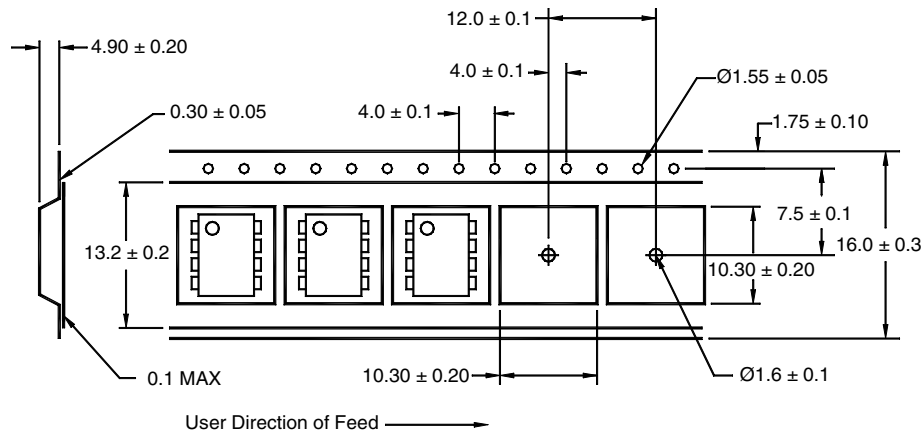
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ORDERING INFORMATION

Option	Order Entry Identifier	Description
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
W	.W	0.4" Lead Spacing

QT Carrier Tape Specifications ("D" Taping Orientation)



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